Towards Sustainable Electronic Design Automation Flow: A Joint Approach Based on Complexity Metrics

Virginie Delalot
INNOVA Advanced Technologies
2 Rue Emile Augier
38000 Grenoble, France
virginie@innova-advancedtech.com

Chouki Aktouf
INNOVA Advanced Technologies
2 Rue Emile Augier
38000 Grenoble, France
chouki@innova-advancedtech.com

Gilles Fritz
INNOVA Advanced Technologies
2 Rue Emile Augier
38000 Grenoble, France
gilles@innova-advancedtech.com

Bastien Gratreaux
INNOVA Advanced Technologies
2 Rue Emile Augier
38000 Grenoble, France
comm@innova-advancedtech.com

Nermine Ali
Universite Paris-Saclay, *CEA, List*
Palaiseau, France
nermine.ali@cea.fr

Lilia Zaourar
Universite Paris-Saclay, *CEA, List*
Palaiseau, France
lilia.zaourar@cea.fr

Abstract—**This paper addresses sustainability criteria and Electronic Design Automation (EDA) needs. We aim to optimize the operational stages of an EDA Flow and address a series of investigations to reduce carbon footprint. Our main purpose is to optimize the design flow, considering sustainability criteria to reduce the environmental impact of EDA tools. First, metrics correlating sustainability and design project complexity are provided and implemented as part of an EDA design solution, which INNOVA Advanced Technologies proposes. Second, the INNOVA design solution provides job scheduling based on sustainability criteria. Typical case studies are provided in this paper.**

Index Terms—EDA, Sustainability, Eco-design.

I. INTRODUCTION

In recent years, the global drive toward an environmentally sustainable society has increasingly relied on advancements in the semiconductor industry. Historically, this industry has prioritized making chips smaller, faster, and more energy efficient, often overlooking environmental impacts.

The rapid increase in chip production is responsible for considerable environmental effects, including the environmental impacts of the different design phases [1]. Hence, the ecological dimension of a chip design is becoming strategic. Therefore, the association of eco-design metrics with traditional power/performance/area (PPA) design metrics is no longer optional for next-generation integrated circuits.

As computing technology and digital accessibility continue to expand, the carbon footprint of the Information and Communication Technology (ICT) sector—measured in *CO*2 emissions—is projected to exceed its current 1.2-2.4% share of global emissions [2]. In 2022 alone, there was a significant rise in digital adoption, with 192 million new internet users, 85 million new mobile phone users, and 300 additional hyperscale data centers expected to be operational by 2024 [3].

Indeed, in digital and electronics in general, it is known that the most polluting stages are the extraction and production of raw materials. The production of most of our mobile phones, computers, and televisions accounts for almost 80% of the greenhouse gas emissions that these devices will produce during their lifetime [4]. Some studies deal with the life cycle as a whole and focus on these stages [5] [6] [7] [8] or on recycling and reuse [9] [10]. However, upstream, the design of electronic components also has an impact, and notions of ecological impact can also guide the choices made for this design. Indeed, there are no small savings when it comes to environmental footprint.

Despite advances in technology scaling and Electronic Design Automation (EDA) that have led to the creation of energy efficient VLSI systems, the overall environmental impact has continued to rise over the past decade. This increase is primarily due to the carbon emissions associated with chip design and manufacturing, known as the embodied carbon footprint. To reduce the environmental footprint of electronics and computing devices, it is essential to develop new tools that enable designers to make informed sustainability decisions throughout the design process. Every step, from EDA tools and design flows to manufacturing, is crucial in enhancing sustainability.

The future of electronics lies in sustainable EDA and manufacturing steps. This approach prioritizes reducing environmental impact and maximizing energy efficiency throughout the product life cycle. Incorporating eco-friendly principles into EDA tools empowers engineers to design

electronic circuits with lower power consumption, sustainable materials, and optimized resource utilization. This approach directly tackles the pressing issue of electronic waste (e-waste) and associated carbon footprints, ensuring adherence to evolving environmental regulations and promoting responsible business practices. Moreover, sustainable EDA facilitates environmentally conscious and socially responsible product development.

Today, typical System on Chips (SoC) design projects can involve the efforts of tens to even hundreds of engineers, with an average project design time of nine to twelve months [11]. Costly design resources are usually required: design automation tools and libraries, third-party intellectual-property cores, and computing server farms for data and design jobs processing. Another equally critical component is the increased focus on sustainability and, more precisely, design resource management: the need to adopt more environmentally responsible design practices. In parallel, during the design of complex chips, cost reduction is becoming a real challenge for small, medium, and large companies. Resource management is a key to containing design cost [12].

However, despite the growing pressure among stakeholders to control the environmental effects of chip design, no standards or international agreements to formalize these mitigation efforts have yet been established. Nevertheless, in line with ISO environmental recommendations [13], eco-design in the microelectronics industry must consider the impact of the full life cycle and adopt a systematic approach to design, especially for complex systems such as SoCs.

With climate change accelerating, it is important to measure and reduce the environmental impact of all areas of human activity. This is particularly true for the production of electronic components, as the number of electronic devices has increased enormously in recent decades; this trend looks set to continue [4] [14], and the planet's resources are limited. Recently, various studies have presented several sustainability methods and approaches in electronics and semiconductors. However, most of the scientific contributions target electronic product life cycles.

The main methodology and criteria for measuring the impact of a product or service is Life Cycle Assessment (LCA). This involves analyzing various stages in their life, from design to end-of-life, via the extraction of raw materials, production, distribution, and use. It enables us to identify the environmental impact stages (consumption of fossil resources, consumption of rare earths, greenhouse gas emissions, water consumption, pollution of natural environments, etc.) and to find solutions to reduce this impact. Life-cycle analysis involves many players throughout the product value chain, such as the various service providers and suppliers, and even beyond, by including consumers or users, right through to recovery and recycling. Nevertheless, these studies need to address the impact of EDA tools and flow for chip design on the process itself.

Inspired by the principles of environmental sustainability—namely *"reduce"* and *"reuse"*—this work explores the potential for creating a Sustainable EDA flow. We propose tools incorporating sustainability considerations in chip design through optimal design space exploration with environmental impact as a key criterion and within the EDA flow. Our approach combines complexity metrics with strategies to reduce the computational effort involved in designing each component of the SoC.

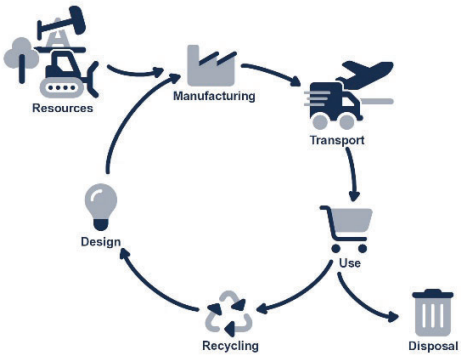

Fig. 1. Life Cycle Assessment.

We introduce *SoC Planner*, a concept to develop a new generation of design exploration solutions for modern System on Chips in a collaborative project. The main objective is to push the design one step further through automation and optimal planning for efficiency in the design process. This project intends to help in the automatic exploration and optimization of SoC design configurations based on several criteria, such as power, performance, and area, by considering the ecological dimension during the design process.

Energy consumption analysis directly impacts climate change. Such analysis correlates to selecting and assigning design resources when starting a new design project. This is particularly true for integrated circuits with large production volumes. During the chip design process, computing servers are used that have a high calculation capacity and significant power consumption of several megawatts per design flow execution. Each tool used for design, verification, or simulation might need to be used for several days, significantly impacting power consumption. Further, many tasks — up to 20% — can fail without yielding convincing results. Climate change mitigation requires using all possible means to avoid wasting energy, especially on tasks that may prove useless.

This paper is organized as follows. Section II presents an in-depth SoC Planner project detailing its primary tools and functionalities. Section III exposes the INNOVA EDA solution for metrics evaluation, followed by Section IV, which discusses the scheduling and allocation of resources based on eco-design criteria. Finally, Section V concludes the paper and discusses future works.

II. SOC PLANNER

With the miniaturization of components, transistor density is increasing faster than the productivity of system-on-chip designers and the improvement of EDA tools. Therefore, the

SoC Planner Project aims to provide system-on-chip designers with a solution to the explosion in design costs, particularly for advanced nodes. This project intends to develop an innovative and indispensable reference software suite for all hardware designers, enabling automatic configuration and planning of the next generation of system-on-chips, guaranteeing the best compromise regarding cost, performance, and eco-design criteria.

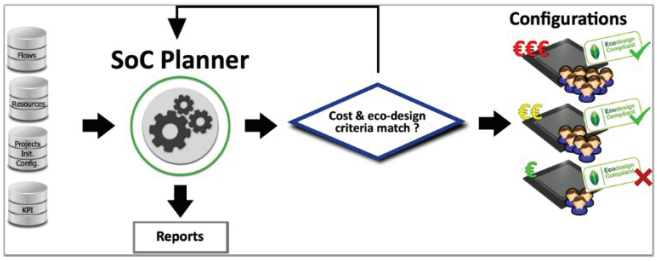

Fig. 2. SoC Design Planning with Sustainability Measures.

The main novelty of the *SoC Planner* project is to limit the number of possible configurations for a complex system-on-chip from the very start of a new design project. It is usual to have hundreds of thousands or even millions of possible configurations for a single project. *SoC Planner* innovation will drastically reduce this number to a set of relevant configurations in line with the scope of the designer specifications at early stages. This will significantly reduce the number of design cycles (iterations of the product development) and, consequently, in development cost savings. An eco-design dimension is also taken into account to enable precise measurement of environmental impact at the start of a new system-on-chip design project, and the minimization of this criterion in the same way as the usual performance criteria (consumption, time, surface area).

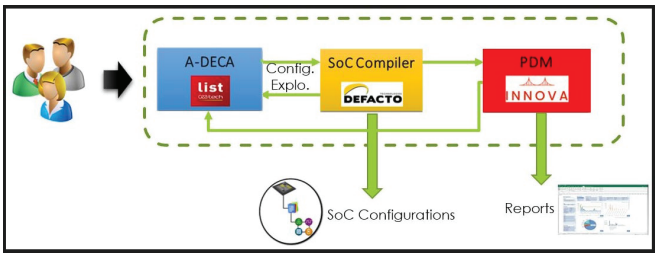

Fig. 3. SoC Planner design flow.

SoC Planner addresses sustainability at the early stages of SoC design by integrating eco-friendly principles throughout every step of the design process. It starts with the ADECA (Automated Design space Exploration for Computing Architectures) tool, which automates the exploration and optimization of computing architecture designs to find the most suitable configurations and guides designers toward more energy-efficient and resource-aware solutions. Next, thanks to the SoC Compiler tool, we automate the generation of RTL and the integration of IPs into a larger SoC, streamlining this process and reducing errors. Finally, the design flow optimization is achieved through INNOVA Project Management (PDM), the design management platform that helps reduce costs by simplifying flow and resource management for SoC and complex electronic systems. The following sections detail the tools: SoC Compiler, A-DECA, PDM.

A. A-DECA framework:

A-DECA aims to address the complexity involved in designing many-core processors by using a modular and automated methodology for the exploration of design parameters [15].

This methodology concentrates on several key aspects by breaking down the challenges of designing and optimizing a complex computing architecture into distinct domains, each equipped with suitable representations and tools to address its specific sub-problem. A-DECA is implemented to be modular and versatile, not restricted to a specific set of parameters imposed by the simulator. Its modularity allows it to adapt to different architectural requirements, ensuring its relevance across diverse applications from High-Performance Computing to Artificial Intelligence IPs and embedded systems. Integrating eco-design principles emphasizes sustainability, guiding the design process to minimize environmental impact while maintaining high performance. Here are the key features of its implementation:

A-DECA places a strong emphasis on sustainability by incorporating eco-design principles. A-DECA inherently promotes sustainability and environmental friendliness by focusing on configurations that minimize area and reduce energy consumption. This approach ensures that the resulting processors are powerful and efficient and align with eco-friendly design principles, reducing their overall ecological footprint and aligning technological advancements with environmental stewardship.

B. SoC Compiler

Defacto Technologies proposes a front-end SoC integration tool called SoC Compiler [16]. It is a software gamechanger for front-end SoC design. This platform addresses the challenges of integrating increasingly complex SoCs with a high level of automation, all before the logic synthesis stage. It excels at managing a multidimensional design flow, considering various aspects like RTL code, pre-designed IP blocks (described by IP-XACT), timing constraints, power consumption, physical layout plans, and test requirements. This unified approach ensures that the SoC design considers all these factors, leading to a more optimized and robust end product at the early stages. This tool provides significant advantages, including achieving optimal Power-Performance-Area (PPA) targets within tight schedules. It accomplishes this through extensive automation of SoC integration tasks before logic synthesis. SoC Compiler promotes design reuse of up to 90% by leveraging existing RTL code and design collateral. Its integration with existing EDA

tool flows is facilitated through support for high and low-level APIs in different programming languages (Tcl, Python, Perl, C++, Java). This software enables SoC creation even in incomplete design blocks or views. SoC Compiler is used most of modern chip design, offering a sophisticated and efficient path to design highly integrated, performance-optimized, and reliable circuits for various applications, including automotive systems and industrial devices. Its ability to establish complex design processes is a key element in advancing integrated circuit technology.

C. Project and Design Management (PDM) solution

INNOVA's Project and Design Management (PDM) is a unified software platform integrating project management presented in figure 4, design flow, and resource management into a single software environment. PDM is thus multi-user, opening to a wide audience: design project managers, design engineers, purchasing departments, and human resources. INNOVA's PDM provides the infrastructure to track the usage of different resources (EDA tools, servers, engineering resources, libraries, etc.). It can be securely plugged into any existing IT environment and inter-operates with standard project, license, and server management tools [17].

INNOVA approach is to provide automated measures, which help detect and filter design and resource configuration that directly impact power consumption and design project sustainability in general. INNOVA PDM design solutions measure if sustainability conditions are fulfilled and help differentiate between different configurations. Configuration means design options, resource options, and design flow altogether. Therefore, the functionalities and access rights to PDM are distributed between these users. PDM key features are summarized as follows:

- It is scalable or extensible, that is to say, it is easily interfaced with existing information systems;
- It ensures consistent data throughout the life of a project, including design information, design assets, design flows, and proprietary project management tools;
- It ensures real-time synchronization with design data.

Being fully compatible with existing software, such as user selected design software and directory management software, PDM serves as a single portal, thereby reducing the complexity of using dedicated design tools and environments. This platform is based on a unique representation model of the different entities handled (software, flows, servers, project, human resources), which ensures interoperability between the three key areas: management of design flows, management of resources, and project management. In addition, this technology can integrate both software aspects, such as design software licenses, and hardware aspects, such as calculation servers, particularly regarding flow management and control. Design entities can include a project, a design stream, design data, or a design resource, such as a server or a license for design software. The design process for a complex SoC requires unified project management, with strong links among the entities involved (see figure 4). Such a management process allows full traceability of the use of design resources.

Therefore, integration with PDM contributes to achieving the overall design flow optimization goals, as presented in the next section.

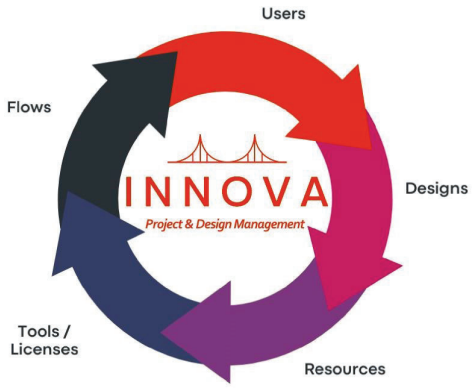

Fig. 4. Innova Unified Design and Project Management design environment.

III. ECO-DESIGN AND SUSTAINABILITY METHODOLOGY BASED ON PDM

INNOVA initiated the work to develop the eco-design and sustainability methodology, which will be validated and adopted during the "*SoC Planner*" project. This methodology is based on the following structuring elements:

- The development of an ecological footprint that will represent a decision-making aid for designers of complex SoCs;
- The prediction of failure or success of design tasks using a learning engine which will limit the waste of resources due to the launch of design tasks whose probability of success is quite low;
- The allocation of resources taking into account eco-design criteria;
- Mapping and Scheduling of design tasks taking into account eco-design criteria.

A. Generation of an ecological footprint/score

The generation of an ecological footprint accompanying the different design stages is at the heart of the eco-design methodology of INNOVA'PDM. Such a footprint will help design engineers make task launch decisions related to the impact of resource consumption and, therefore, energy. It is noteworthy that PDM already provides several complexity metrics that target design configuration, design flow configuration, design resource configurations, etc. An adequate combination of these metrics reflects a project's complexity. It provides a meaningful score to deem an SoC project highly,

medium, or low complex. This directly impacts the project's sustainability and its related impact on power consumption. We illustrate these metrics here through the typical use case presented below.

B. Typical Case Study – Flow complexity metrics

The flow complexity metric is part of other metrics of an overall sustainability score. This score is considered to compare the complexity of different design projects. Here, the focus is on design flows and their related complexity. The main objective is to be able to compare different versions of the same design flow. In other words, for one design flow, how complex are the changes if we decide to split or partition a complex SoC design into 2, 3, 4, or 5 partitions/parts towards logic synthesis.

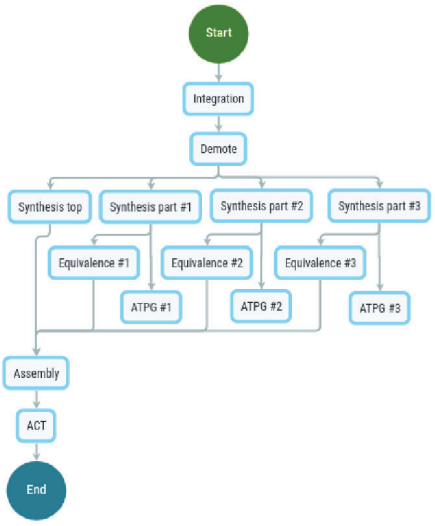

Fig. 5. Typical flow use cases for multi-partitions SoC design.

Designers know this as parallel vs. serial synthesis. Two different metrics are computed: cyclomatic complexity and N-path metrics. These two metrics reflect the graph complexity for design flows. Table I below provides the related complexity values. The first column gives the number of steps, and the next two are the metrics Cyclomatic complexity and N-Pat, respectively.

TABLE I

DESIGN FLOW : COMPLEXITY METRICS.

Metrics:	Cyclomatic complexity	N-Path
2 parts	7	10
3 parts	9	22
4 parts	11	50
5 parts	13	114

As we can see in the graph of Figure 6 below, several parts directly impact the flow complexity: as expected, cyclomatic complexity shows that we increase the number of linearly independent paths - each new part adds two linearly independent paths; N-path shows that we have increased number of possible paths exponentially. Indeed, a new step has two potential paths, success or failure, multiplied by other possible paths. Finally, the weighted average shows that the needed resources are directly proportional to the number of parts.

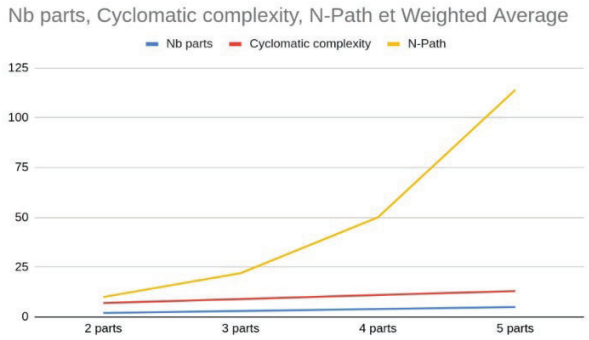

Fig. 6. Evolution of complexity compared to number of parts and number of paths.

IV. SCHEDULING AND ALLOCATION OF RESOURCES BASED ON ECO-DESIGN CRITERIA

Traditionally, design tasks are executed according to the rule of *"First In, First Out"* without any consideration of the availability of resources (servers, design software licenses, etc.). INNOVA PDM shortens the execution times of design tasks thanks to optimized management of resources (licenses, servers), reducing waiting times to access such resources. Thus, by having an overall view of the tasks to be executed and their need in terms of resources, it is possible to schedule these tasks in such a way as to reduce blockage scenarios and bottlenecks due to lack of resources, as illustrated in the figure 7 below. Indeed, the first schedule takes the tasks in the arrival order (red, blue, then yellow) and executes them as soon as resources are available. The second one identifies that executing the red tasks first induces long waiting times and will focus on implementing the blue tasks first. One of the key points for task scheduling to be most effective is estimating the duration of a task. INNOVA's PDM, through automatic learning from previous executions, is a central element for the automatic estimation of task execution time.

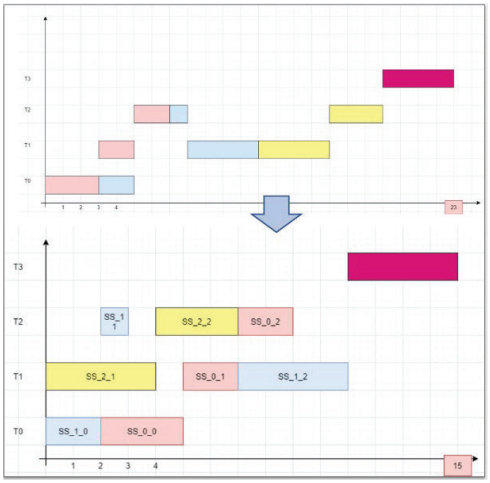

Fig. 7. Automated management of design tasks and jobs based on resource availability.

As illustrated in figure 7, when design jobs are executed based on available resources, the resources consumed during a design project will be positively impacted. For example, a longer execution for the logic synthesis design step (usually called silicon compilation) can mobilize up to ten servers, which results in a consumption of around $40kWh$. Consumption management at all levels will thus enable significant energy performance for complex digital integrated circuits. With a global view of the design tasks and the resource requirements, design decisions can be made based on resource availability, yielding more predictable project outcomes. Such visibility opens new options for design and resource allocation and scheduling, with the ability to modify the list of design tasks and shift or cancel unnecessary ones. Managers can now order design tasks based on resource availability and define the priorities for each task. Design managers and decision-makers can focus design teams on those tasks related to higher-priority and strategic projects.

V. CONCLUSION

The future of electronics lies in sustainable EDA and manufacturing steps. In this work, we incorporate eco-friendly principles into EDA tools to empower engineers in the design of electronic circuits with lower power consumption, sustainable materials, and optimized resource utilization. In a collaborative project, we introduce *SoC Planner*, a concept to develop a new generation of design exploration solutions for modern System on Chips. The main objective is to push the design one step further through automation and optimal planning for efficiency in the design process. Modern project management methodologies are required to address current resource management challenges during the SoC design process, enabling design entities to manage design projects jointly and with the resources necessary. Beyond cost, eco-design is a dimension of SoC design that EDA tools can no longer ignore. This work has presented a new EDA design approach and solution that considers sustainability key when qualifying an SoC design project. The strategy is structured around complexity metrics and job scheduling based on resource availability criteria. As a perspective for this work, new metrics will be added to the current INNOVA design solution.

ACKNOWLEDGMENT

The SoC Planner Project has received funding from the French institution BPI France.

REFERENCES

[1] G. Marinova and A. Bitri, "Challenges and opportunities for semiconductor and electronic design automation industry in post-covid-19 years," *IOP Conference Series: Materials Science and Engineering*, vol. 1208, p. 012036, 11 2021.

[2] M. G. Bardon, P. Wuytens, L.-A. Ragnarsson, G. Mirabelli, D. Jang,˚ G. Willems, A. Mallik, A. Spessot, J. Ryckaert, and B. Parvais, "Dtco including sustainability: Power-performance-area-costenvironmental score (ppace) analysis for logic technologies," in *2020 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2020, pp. 41–4.

[3] J. C. Herlin, "Kaupunkimarkkinointi tiktokissa," 2022.

[4] (2020 - 2023) Ademe-arcep study: assessment of the digital environmental footprint in france in 2020, 2030 and 2050. [Online]. Available: https://en.arcep.fr/uploads/tx gspublication/press-kit-study-Ademe-Arcep-lot3 _march2023.pdf

[5] T. Pirson, T. P. Delhaye, A. G. Pip, G. Le Brun, J.-P. Raskin, and D. Bol, "The Environmental Footprint of IC Production: Review,Analysis, and Lessons From Historical Trends," *IEEE Transactions on Semiconductor Manufacturing*, vol. 36, no. 1, pp. 56–67, Feb. 2023, conference Name: IEEE Transactions on Semiconductor Manufacturing. [Online]. Available: https://ieeexplore.ieee.org/document/9979766

[6] B. Li, R. B. Roy, D. Wang, S. Samsi, V. Gadepally, and D. Tiwari, "Toward Sustainable HPC: Carbon Footprint Estimation andEnvironmental Implications of HPC Systems," in *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*, Nov. 2023, pp. 1–15, arXiv:2306.13177 [cs]. [Online]. Available: http://arxiv.org/abs/2306.13177

[7] S. B. Boyd, *Life-cycle assessment of semiconductors*. University of California, Berkeley, 2009.

[8] F. Taiariol, P. Fea, C. Papuzza, R. Casalino, E. Galbiati, and S. Zappa, "Life cycle assessment of an integrated circuit product," in *Proceedings of the 2001 IEEE International Symposium on Electronics and the Environment. 2001 IEEE ISEE (Cat. No.01CH37190)*, 2001, pp. 128–133.

[9] U. Gupta, M. Elgamal, G. Hills, G.-Y. Wei, H.-H. S. Lee, D. Brooks, and C.-J. Wu, "ACT: designing sustainable computer systems with an architectural carbon modeling tool," in *Proceedings of the 49th Annual International Symposium on Computer Architecture*, ser. ISCA '22. New York, NY, USA: Association for Computing Machinery, Jun. 2022, pp. 784–799. [Online]. Available: https://doi.org/10.1145/3470496.3527408

[10] C. Fitzpatrick, J. Walsh, and I. Grout, "Environmentally superior implementation of electronic hardware through modular programmable logic devices & eco design," in *Proceedings of the 2006 IEEE International Symposium on Electronics and the Environment, 2006.*, 2006, pp. 228– 232.

[11] J. A. Darringer, R. A. Bergamaschi, S. Bhattacharya, D. Brand, A. Herkersdorf, J. K. Morrell, I. I. Nair, P. Sagmeister, and Y. Shin, "Early analysis tools for system-on-a-chip design," *IBM Journal of Research and Development*, vol. 46, no. 6, pp. 691–707, 2002.

[12] T. Li, J. Hou, J. Yan, R. Liu, H. Yang, and Z. Sun, "Chiplet heterogeneous integration technology—status and challenges," *Electronics*, vol. 9, no. 4, 2020. [Online]. Available: https://www.mdpi.com/2079-9292/9/4/670

[13] International Organization for Standardization (ISO): Geneva, Switzerland, "Iso 14001:2015; environmental management systems - requirements with guidance for use." 2015. [Online]. Available: https://www.iso.org/standard/60857.html

[14] F. Bordage. (2019) The environmental footprint of the digital world. [Online]. Available: https://www.greenit.fr/wp-content/uploads/2019/11/GREENIT EENM etude EN accessible.pdf

[15] L. Zaourar, A. Chillet, and J.-M. Philippe, "A-DECA : an Automated Design space Exploration approach for Computing Architectures to develop efficient high-performance many core processors," in *DSD/SEAA 2023 - 26th Euromicro Conference Series on Digital System Design (DSD) and 49th Euromicro Conference Series on Software Engineering and Advanced Applications (SEAA)*, Durres, Albania, Sep. 2023, pp. 756–763. [Online]. Available: https://cea.hal.science/cea-04224485

[16] Front-end soc integration. [Online]. Available: https://defactotech.com/products-solutions/soc-integration-at-rtl

[17] [Online]. Available: https://www.innova-advancedtech.com/