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A Low-Power ADC-Free Resistive Sensor Readout Circuit for µC-Based Microsystems

João Maia Aguiar
INESC TEC, Faculdade de Engenharia
Universidade do Porto
Rua Dr Roberto Frias, 4200-465 Porto, Portugal
joao.m.aguiar@inesctec.pt

José Machado da Silva
INESC TEC, Faculdade de Engenharia
Universidade do Porto
Rua Dr Roberto Frias, 4200-465 Porto, Portugal
jms@fe.up.pt

Abstract — **Implantable microsystems are required to show low-volume and low-power consumption, while ensuring high reliability and safe long-term operation. This work addresses the development and evaluation of a compact readout circuit for a piezoresistive force sensor intended for integration in an active oral prosthesis. The approach proposed here can be included in the direct-to-microcontroller interface methodologies, but relies on a sigma-delta-like measurement process. Its performance has been experimentally compared to conventional Wheatstone bridge and simple voltage-divider topologies, showing, respectively, 76% and 44% reductions in power consumption, while ensuring 8 times better resolution.**

Keywords- Resistive sensor; ADC-free readout; low-power.

I. INTRODUCTION

The oral cavity plays an essential role in mastication, swallowing, speech, and postural regulation. Teeth, muscles, temporomandibular joints, and the nervous system act together to regulate masticatory bite force, depending on the sensory feedback from oral mechanoreceptors, particularly periodontal mechanoreceptors. These detect force, direction, and duration of tooth loading and transmit this information to the central nervous system [1,2]. This feedback is essential for efficient chewing and to prevent excessive mechanical stress. Tooth loss reduces or eliminates the natural periodontal feedback pathway, leading to reduced perception of biting and chewing forces. Excessive masticatory loading has been associated with fixed-prosthesis complications, including ceramic fracture, screw loosening, peri-implant bone loss, and premature implant failure [2,3].

The application targeted here concerns the development of an active oral prosthesis, featuring pressure-sensing and stimulation circuits meant for sensory feedback restoration. Biofeedback-based approaches have already been explored for managing masticatory muscle activity in awake bruxism [4], but no developments have been proposed regarding the restoration of biting and chewing proprioception. Embedding a sensing and stimulation electronic microsystem within such a prosthesis imposes severe constraints on its characteristics: it must be compact, thermally safe, and show low-volume/low-power to ensure comfort and integrate easily into the prosthesis.

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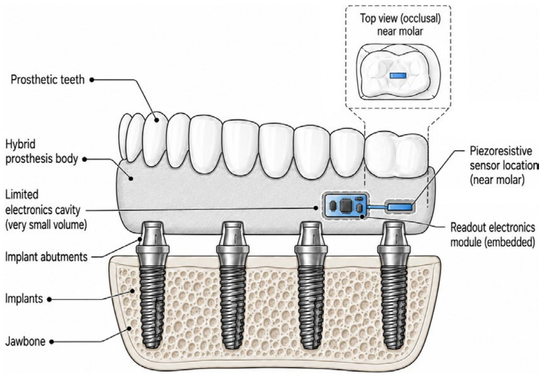

Figure 1. Proposed active prosthesis, showing the placement of the force sensor and readout electronics.

Fig. 1 illustrates the integration scenario being considered in this work. For the pressure-sensing stage, piezoresistive sensors are being used due to their simple structure, small size, and direct resistance variation under mechanical load. The sensor being used is a HAPTICA semiconductor strain gauge integrated on a flexible substrate, with nominal resistance of $5 \pm 0.5\ k\Omega$, dimensions of $\approx 1.524 \times 0.838 \times 0.203\ mm^3$, and a specified gauge factor of $GF = 175 \pm 10$. Its reduced size, flexible support, and high sensitivity make it suitable for integration in the prosthesis structure being designed.

Conventional resistive sensor interfaces often rely on constant voltage Wheatstone Bridge (WB) and simple resistive voltage divider (VD) configurations. However, these topologies imply: the former ones, the need for extra high-accuracy components, high-resolution analog-to-digital converters (ADCs), an instrumentation amplifier; the second ones show lower sensitivity and higher susceptibility to supply voltage noise and loading errors, and allow for the use of single-ended ADCs. Also, lower power consumption can be achieved with VD if a high series resistance is used, but eventually that implies the need for a low-power signal amplification stage prior the ADC to ensure the required dynamic range is captured [5]. Current biased WB and VD sensor interfaces can be adopted, but these imply extra circuitry to implement the current source.

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TABLE I. CHARACTERISTICS AND FEATURES OF RESISTIVE SENSOR ADC-FREE READOUT CIRCUITS.

Ref.	# Components	Resolution	Sensitivity	Sensor Range
[12]	8	20 counts/Ω	0.05 Ω at 1 MHz	1–19 Ω
[13]	8	20 counts/Ω	0.05 Ω at 1 MHz	0.5 kΩ–4.5 kΩ
[14]	10	32.8 counts/Ω	0.03 Ω at 656.25 kHz	80–150 Ω (Pt100), 1 kΩ–1 MΩ (Pt1000)
[15]	9	—	Current boosting (21.1–49.4×)	3.63 kΩ–488.2 kΩ
[16]	9	—	Resistance-to-time conversion	RTD equivalent range
[17]	4	8-bit	Adaptive DAC-based readout	Conductive polymer gas sensors
[this work]	3	42.3 Ω	165 μV / Ω	4700 – 5250 Ω
Ref.	**Error**	**Power**	**Measurement Time**	**Processing Method**
[12]	0.022%	—	60 ms	10–12 MCU operations
[13]	0.18%	—	13 ms	10–12 MCU operations
[14]	0.29%	12 mW	15 ms + 3 discharge times	10–11 MCU operations
[15]	±0.28%	0.275 mW–2.03 μW	4.78 ms – 389.3 ms	Dual-slope timing sequence
[16]	0.11%	—	2 charge-discharge cycles	MCU timing measurement
[17]	—	86.41 μW @ 1 V	Adaptive conversion	8-bit UP/DN counter
[this work]	0.5%	1.32 mW @ 3.3 V	20 ms (depending on averaging window)	MCU relative timing measurement

In microcontroller (μC) –based systems, one can take advantage of the embedded ADC to reduce the external circuitry. Nevertheless, the typical power consumption of ADC embedded in commercial μC varies from sub-mW to few mW per conversion, depending on the operating frequency, building technology, and number of conversion bits [6 – 8].

Alternative methods can be divided into resistance-to-frequency converters, resistance-to-phase converters, and direct interface circuits (DIC), all of them relying on a digitization process carried out by a μC timer that performs a time-to-digital conversion [9]. The resistance-to-frequency and resistance-to-phase conversion methods often require additional passive and active elements like oscillators, operational amplifiers, voltage references, switches, or logic gates [8 – 11]. In the DIC-like cases, the resistive sensor is directly connected to the μC, being the measurement process based on the charge-discharge (C/D) timing of a capacitor, eventually involving some other resistors and multiple conversion cycles.

Table I lists representative resistive sensor interfacing circuits and highlights the reported respective characteristics and design trade-offs. The methods in [12] and [13] rely on resistance variable frequency oscillators, using a μC counter to obtain the oscillation frequency, i.e., the time taken to C/D a capacitor. [14] extends this principle to improve robustness against lead-wire resistance, but now, opposed to presetting the C/D duration, the proposed scheme configures and adapts the respective periods to perform the measurement. The self-heating-compensated digitizer described in [15] focuses on limiting sensor power dissipation through low excitation currents and current boosting, resorting to a dual-slope integrator and a comparator to generate a time sequence output signal, which is directly fed to the digital pin of a μC for time counting. The enhanced resistance-to-time interface in [16] targets faster conversion and lead-wire compensation using a reduced number of C/D cycles at the cost of a more complex external circuit involving a multivibrator, a set of switches, and diodes, to impose different C/D paths. Finally, in [17] the ADC-free adaptive interface uses a feedback-controlled counter/DAC structure to compensate baseline drift and reduce power in gas-sensor applications.

The next section describes the operating principle of the proposed approach. Section III presents the setups used to evaluate and compare its performance. The results are discussed in Section IV, and final conclusions are provided in Section V.

II. THE ΣΔ-BASED DIC APPROACH

Compared to the approaches listed in Table I, the scheme proposed here prioritizes lower hardware complexity and power consumption, rather than maximum resolution or lead-wire compensation. The scheme in Fig. 2 shows its principle of operation. The sensor R_S is connected between a reference voltage V_{Ref} and the μC digital input port P_i. Capacitor C connects between P_i and Ground. The auxiliary resistor R_F is connected between P_i and the digital output port P_o. During the measurement time T_m, several C charge and discharge cycles are performed. To achieve that, v_{Fed} is switched high (V_{DD}) when the capacitor voltage v_C reaches the V_{IL} voltage (lower limit) of P_i, forcing C to start a new charging cycle; when v_C reaches the P_i's V_{IH} voltage (upper limit) the output v_{Fed} is switched low (Ground) forcing C to start a new discharging cycle.

During each C/D cycle, a counter, operating at a higher frequency, is used to measure the respective time. Once the measurement time T_m is accomplished, the average value of voltage v_{Fed} (V_{Mes}) is calculated as in (1),

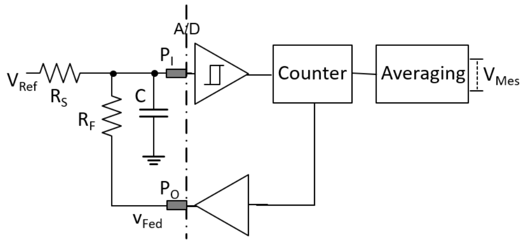

Figure 2. Block diagram of the direct-interface scheme proposed here.

$$< v_{Fed} > = V_{Mes} = V_{DD} \times \frac{N_c}{N_c + N_d} \tag{1}$$

where N_c is the total number of sampling periods counted during charging cycles, and N_d is the total number of counts during discharging cycles. This process is similar to that of a first-order ΣΔ A/D conversion process. In each instant, the capacitor current is given by the differential equation

$$C\frac{dV_C(t)}{dt} = \frac{V_{Ref} - V_C(t)}{R_S} + \frac{V_{Fed} - V_C(t)}{R_F} \tag{2}$$

whose solution is $v_c(t) = V_{Fin} + [Vc(0) - V_{Fin}]e^{-t/(R_{eq}C)}$, where R_{eq} is the parallel of R_S and R_F and V_{Fin} is either V_{DD} or *Ground*. The feedback loop operates by seeking to cancel the error that occurs between the instantaneous $v_c(t)$ voltage and the targeted voltage given by the voltage divider

$$V_\infty = \frac{V_{Ref}R_F + V_{Fed}R_S}{R_F + R_S}, \tag{3}$$

which is the midpoint swing of the input P_i logic comparator, typically ≈ $V_{DD}/2$ — this value has to be adjusted after calibration. Therefore, the V_{Ref} and R_{eq} values have to be selected so that the final capacitor voltage V_{Fin} is higher than the midpoint threshold in the charging cycle and lower in the discharging cycle. Once V_{Mes} is known, the sensor resistor is found from

$$R_S = R_F \times \frac{V_{Ref} - \frac{V_{DD}}{2}}{\frac{V_{DD}}{2} - V_{Mes}} \tag{4}$$

Equation (4) shows that for higher detection sensitivity, V_{Ref} should be different from $V_{DD}/2$, either V_{DD} or *Ground* for maximum sensitivity.

III. Methods and Materials

Preliminary validation of the proposed DIC approach was carried out resorting to both simulation and experiments. Previous mechanical tests performed with a sensor embedded in an oral prosthesis subjected to forces from 0 to 400 N showed that the HAPTICA RS resistance varies approximately linearly between 4700 Ω and 5250 Ω.

For this validation, the sensor was emulated with resistors swept in steps of 50 Ω. For each resistance value, twelve measurements were obtained to evaluate the repeatability of the circuit response. All simulations and experiments were performed with a supply voltage of 3.3 V, matching the expected operating voltage of the microcontroller intended for future system integration.

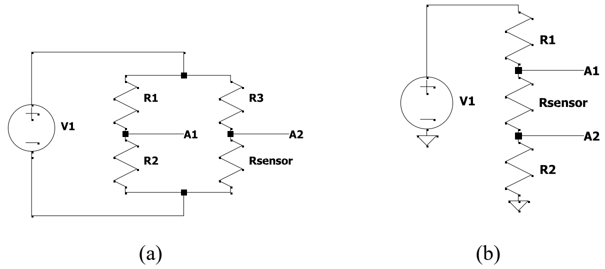

Figure 3. (a) Wheatstone bridge configuration. V1 = 3.3 V, R1 = R2 = R3 = 5.6 kΩ, and Rsensor = 4700 Ω : 5250 Ω. (b) Voltage-divider configuration. V1 = 3.3 V. Alternative scenarios: R1 = 0 and R2 = 4.7 kΩ; R1 = 1 kΩ, R2 = 3.9 kΩ; and R1 = 2.2 kΩ, R2 = 2.7 kΩ.

A. Simulation

All simulations were performed in LTSpice over a 20 ms analysis window. Although no noise source was included at this stage, this duration was adopted to provide enough time to accommodate capacitive transients. In particular, the extended window allowed the charging, discharging, and steady-state behavior of the capacitor to be observed without constraining the analysis to the initial response only. The same time interval was also adopted as a reference for the bench experiments, enabling a direct comparison between simulated and experimental measurements using equivalent observation windows.

A conventional Wheatstone bridge (Fig. 3.a) was used as a control reference. The bridge was implemented using fixed 5.6 kΩ resistors, together with the variable resistor representing the piezoresistive sensor. These resistance values implied a measurement $V_{A1} - V_{A2}$ offset but, on the other hand, allowed reducing the respective power dissipation.

The output voltage of the voltage-divider-based readout configuration (Fig. 3.b), is given by

$$|V_{out}| = |V_{A1} - V_{A2}| = V_{DD}\frac{R_{sensor}}{R_1 + R_{sensor} + R_2} \tag{5}$$

which depends on the sensing resistance and on the total series resistance, $R_1 + R_2$, rather than on the individual values of R_1 and R_2. Therefore, two configurations with the same total series resistance should produce the same differential output behavior. The removal of R_1 was also considered because it reduces the number of components and simplifies the readout structure. Three scenarios were simulated: 1) R_1 = 0, R_2 = 4.7 kΩ; 2) R_1 = 1 kΩ, R_2 = 3.9 kΩ; and 3) R_1 = 2.2 kΩ, R_2 = 2.7 kΩ. In the 2) and 3) cases the total series resistance is 4.9 kΩ.

As for the proposed DIC interface, the circuit shown in Fig. 4 was used, where R_1 = 920 Ω and C = 82 nF, while R_{sensor} was swept from 4700 Ω to 5250 Ω. Two V_{Ref} cases were evaluated, corresponding to V_1 = 3.3 V and V_1 = 0 V.

The circuit was modelled using a comparator with a threshold reference equal to approximately 0.6 V with a hysteresis window width of ≈ 15 mV.

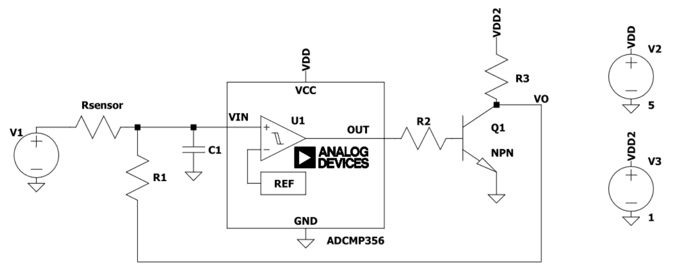

Figure 4. Scheme of the simulated ΣΔ DIC being proposed. $R_1 = 920\,\Omega, C_1 = 82\,nF, R_{sensor} = 4700\,\Omega : 5250\,\Omega$.

B. Experimental setup

For the experimental evaluation, the same nominal resistance range was considered. Instead of the real sensor, arrangements of discrete resistors, with 47 Ω increments, were used to simplify the practical resistor implementation. In all cases, an Arduino Due was used as the readout platform ($V_{DD} = 3.3\ V$). For the WB and VD configurations, the respective $V_{A1} - V_{A2}$ output voltages where captured with the 12-bit ADC built in the ATSAM3X8E ARM Cortex-M3 µC. After performing the WB and VD measurements, an additional test was performed to evaluate the effect of acquisition noise on the measured voltages. For both configurations, the Arduino Due sampled the output at 1 kHz, and the acquired values were processed using a sliding-window average. This was used to study the trade-off between measurement stability and acquisition duration, as shorter acquisition windows can reduce the active measurement time and, consequently, the average power consumption, provided that the output accuracy is not significantly affected. Three additional acquisition settings were tested. The first used a window length of 100 samples with a delay of 1 ms between updates. The second one used a window length of 20 samples with a delay of 5 ms. The third used a window length of 5 samples with a delay of 20 ms. These configurations preserve a comparable overall observation interval while changing the number of samples used in each averaging, allowing for a tradeoff among acquisition time, noise reduction, and measurement stability to be evaluated.

As for the proposed ΣΔ DIC interface case, only the average output voltage was acquired and used for comparison with the simulated response. The same 20 ms observation window was used. However, the first 500 µs were excluded from the average calculation to avoid the initial transient period of the feedback loop. The Arduino Due was configured to acquire the output at the highest sampling frequency achievable with the implemented code, i.e., $f_S \approx 118$ kHz. The current consumptions of all circuits were measured using a current sensor placed in the power supply.

Unlike the simulation model, where the switching threshold was defined by the fixed internal reference of the comparator, the Arduino Due digital input has an undefined transition region in which the logic state is unpredictable. For this reason, the external component values had to be adjusted experimentally. Three configurations were evaluated: $R_1 = 3047\ \Omega$ with $C_1 = 82$ nF and $V_1 = 0$ V; $R_1 = 2047\ \Omega$ with $C_1 = 82$ nF and $V_1 = 3.3$ V; and $R_1 = 2027\ \Omega$ with $C_1 = 82$ nF and $V_1 = 3.3$ V. These values were selected after studying the maximum usable value of R_1 for each input-source condition. The objective was to increase the output voltage variation while avoiding operation inside the undefined digital-input transition region. For $V_1 = 3.3$ V, the maximum evaluated value was $R_1 \cong 2044\ \Omega$, resulting in an output variation of about 385 mV. For $V_1 = 0$ V, the maximum evaluated value was $R_1 \cong 3056\ \Omega$, resulting in an output variation of about 460 mV.

TABLE II. SUMMARY OF SIMULATION RESULTS.

Configuration	Output Range [V]	Total Variation [mV]	Minimum Step [mV]
Wheatstone bridge	0.144 – 0.053	91	8
VD, R_2 = 4.7 kΩ	1.650 – 1.741	91	8
VD, R_1 =1 kΩ, R_2 = 3.9 kΩ	1.616 – 1.707	91	8
VD, R_1=2.2 kΩ, R_2=2.7 kΩ	1.616 – 1.707	91	8
ΣΔ DIC, V_1 = 3.3 V	0.053 – 0.109	56	5
ΣΔ DIC, V_1 = 0 V	0.690 – 0.678	12	1

IV. RESULTS AND DISCUSSION

As can be seen from Fig. 3 and 4, the number of external components used in each case are: 4 ($R_{sensor}, R_1, R_2, R_3$) for the WB, 2/3 ($R_{sensor}, R_2\ /\ R_1$) for the VD, and 3 ($R_{sensor}, R_1, C_1$) for ΣΔ-based DIC.

A. Simulation results

The output voltages obtained after simulation of the three topologies are summarized in Table II. In each case, the output range, total voltage variation, and minimum voltage step were extracted to compare the simulated readout behavior.

For the WB configuration, the output voltage decreased from approximately 144 mV at 4700 Ω to 53 mV at 5250 Ω, corresponding to a total variation of about 91 mV. The absolute voltage step between consecutive resistance values ranged approximately from 7.9 mV to 8.7 mV.

The VD configurations produced higher absolute output voltages, ranging from approximately 1.650 V to 1.741 V for the configuration with $R_2 = 4.7$ kΩ. The total voltage variation was approximately 91 mV, similar to the Wheatstone bridge. The two configurations with $R_1 + R_2 = 4.9$ kΩ produced equivalent results, confirming the prediction of (5). In all VD cases, the voltage step remained close to 8 mV.

For the proposed DIC topology, with $V_1 = 3.3$ V, the average output voltage increased from approximately 53 mV to 109.2 mV, resulting in a total variation of about 56 mV and a minimum voltage step close to 5 mV. With $V_1 = 0$ V, the average output voltage decreased from approximately 690 mV to 678 mV, corresponding to a smaller total variation of about 12 mV and a minimum voltage step close to 1 mV.

B. Experimental results

The experimental results obtained with the Arduino Due readout are summarized in Table III. Overall, the WB and VD configurations followed the same trend observed within the simulations, presenting a nearly linear voltage variation over the emulated sensor resistance range.

TABLE III. EXPERIMENTAL RESULTS.

Configuration	Output Range [V]	Total Variation [mV]	Minimum Step [mV]
Wheatstone bridge	0.156–0.064	92	8
VD, R2 = 4.7 kΩ	1.662–1.753	91	7
VD, R_1=1 kΩ, R_2= 3.9 kΩ	1.627–1.719	92	7
VD, R_1=2.2 kΩ, R_2=2.7 kΩ	1.619–1.711	92	8
ΣΔ DIC, R_1=2047 Ω, V_1=3.3 V	0.556–0.679	123	11
ΣΔ DIC, R_1=2027 Ω, V_1=3.3 V	0.546–0.689	143	13
ΣΔ DIC, R_1=3047 Ω, V_1=0 V	2.284–2.193	91	7

In the WB case, the measured output voltage decreased from approximately 156 mV at 4700 Ω to 64 mV at 5250 Ω, that is, a total variation of about 92 mV, with a minimum absolute voltage step of ≈ 8 mV between consecutive resistance values. For the VD configurations, in the $R_2 = 4.7$ kΩ case, the measured voltage increased from ≈ 1.662 V to ≈ 1.753 V, resulting in a minimum voltage step of ≈ 7 mV. When R_1 was included, similar total variations were obtained, with output ranges of $1.627 - 1.719$ V and $1.619 - 1.711$ V, respectively. These results are consistent with the simulated behavior, where the differential voltage variation remained approximately unchanged for equivalent total series resistance values.

The influence of the acquisition time was also evaluated using the sliding-window settings described in Section III-B. Compared to the main acquisitions, the configurations using 100 samples with a 1 ms delay and 20 samples with a 5 ms delay showed a maximum deviation of $\approx \pm 1$ mV. Shortening the window to 5 samples with a 20 ms time increased the deviation to $\approx \pm 5$ mV. This confirms that shorter averaging windows increase the influence of acquisition noise, although the measured deviations remained within the same order of magnitude as the voltage steps reported for these configurations.

The experimental results followed the same general trend observed in the simulation of the WB and VD configurations. The measurements made with different acquisition windows showed that, as expected, the WB and VD outputs are improved after averaging. The cases using 100 samples and 20 samples produced deviations of $\approx \pm 1$ mV, whereas reducing the window to 5 samples increased the deviation to $\approx \pm 5$ mV. Considering that the voltage step between consecutive resistance values is close to $7 - 9$ mV, very short averaging windows may hinder resistance resolution levels. Thus, the averaging window should be selected according to the required force resolution and power-consumption constraints.

Regarding the ΣΔ-based DIC, the experimentally extracted average output voltage showed a stronger dependence on the selected external component values. With $R_1 = 2047$ Ω, $C_1 = 82$ nF, and $V_1 = 3.3$ V, the average voltage increased from ≈ 0.556 V to ≈ 0.679 V, resulting in a total variation of about 123 mV. Using $R_1 = 2027$ Ω, $C_1 = 82$ nF, and $V_1 = 3.3$ V, the voltage increased from ≈ 0.546 V to ≈ 0.689 V, corresponding to a total variation of about 143 mV. In the configuration with $R_1 = 3047$ Ω, $C_1 = 82$ nF, and $V_1 = 0$ V, the average output voltage decreased from ≈ 2.284 V to ≈ 2.193 V, resulting in a total variation of about 91 mV. This is an aspect that deserves further clarification. Nevertheless, the targeted application may not require discrimination between so closely spaced resistance values.

TABLE IV. POWER SUPPLY CURRENT AND READOUT CIRCUIT POWER CONSUMPTION (V_{DD} =3.3V).

Configuration	Total Current [mA]	Circuit Power [mW]
WB	59.6	5.61
VD	58.8	2.97
ΣΔ DIC	58.3	1.32

Table IV summarizes the measured current consumption of each topology. Since the Arduino Due was used as the readout platform in all experimental tests, its baseline current (≈ 57.9 mA) was subtracted from the total measured current. The three topologies, WB, VD, and ΣΔ based DIC, presented currents of ≈ 1.7 mA, ≈ 0.9 mA, and ≈ 0.4 mA, respectively.

The current measurements further highlight the trade-off between readout simplicity and power consumption during measurement time. The higher current consumption of the WB and VD configurations is expected, since both architectures include continuous resistive paths between the supply and ground. In contrast, the ΣΔ-based DIC relies on feedback-based switching operation and avoids the need for an ADC block, which contributes to the lowest additional current consumption among the three topologies.

The total power consumption depends heavily on the readout platform. We used the Arduino Due because it is convenient and compatible with 3.3 V supply, but it is not designed for ultra-low-power use. Choosing a lower-power µC or a dedicated readout circuit in future versions will reduce power consumption and make the system more suitable for integration into an intraoral prosthesis.

When compared with the approaches summarized in Table I, the proposed circuit follows a different design priority. Several reported resistive sensor interfaces focus on high resolution, lead-wire compensation, or resistance-to-time conversion accuracy. These approaches are suitable for precision instrumentation, but they often require additional timing stages, multiple conversion cycles, or a larger set of external components. In contrast, the present work targets a highly constrained intraoral application, where compactness, low power consumption, and reduced component count are primary requirements. Also, the expected temperature variation range is small and thus compensation for temperature variations is not a critical issue. The proposed ΣΔ-based DIC is not intended to outperform all previous methods in terms of linearity or resolution, but rather to provide a compact readout alternative for a piezoresistive force sensor embedded in an oral prosthesis.

V. Conclusion

This work presented and evaluated different readout circuits for a piezoresistive force sensor, intended for integration in an oral prosthesis. The main objective was to compare simple resistive sensor interfaces under the constraints of reduced size, low power consumption, and compatibility with compact embedded electronics.

A ΣΔ-based direct interface with a µC circuit has been proposed that outperforms the conventional Wheatstone bridge and voltage divider circuits in terms of power consumption and does not require the use of an ADC, while providing similar resolution. Compared to other direct interface circuits the solution being proposed presents a lower component count.

The undefined midpoint swing of the µC digital input port used as a 1-bit quantizer may introduce a non-linearity in the measurement. Nevertheless, the dense resistance sweep used in this study represents a demanding characterization condition, and broader calibration intervals may be sufficient for the targeted intraoral force-monitoring application.

Ongoing work is focusing on improving the precision and monotonicity of the topology being proposed, as well as on replacing the prototyping platform with a lower-power embedded implementation suitable for intraoral prosthetic integration.

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