Study of PicoTDC Performance for FIT Detector Upgrade in ALICE Experiment at CERN

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Abstract—**In this paper, we present the results of a study on the performance of the PicoTDC. PicoTDC is a new Time-to-Digital Converter (TDC) chip developed at CERN for time-of-flight measurements in high-energy physics experiments. Our research aimed to evaluate the feasibility of using the PicoTDC in the upgraded front-end electronics (FEE) of the Fast Interaction Trigger (FIT) detector in the ALICE experiment. The FIT detector provides the trigger signals for the other ALICE sub-detectors and operates under very tight latency constraints. Since the necessary PicoTDC performance data were not available in the published documentation, we decided to derive the required parameters from simulations. The unique contribution of this paper is a detailed explanation of the output signals' timings of PicoTDC. Additionally, we propose a sensor channel allocation scheme that reduces the guaranteed PicoTDC processing time. We derive and present useful analytical formulas for calculating the output latency across different usage scenarios. Finally, we present a case study that assesses the feasibility and the conditions required to meet the latency and data-rate requirements when incorporating the PicoTDC into the upgraded FIT front-end electronics.**

Keywords: PicoTDC, FIT detector, TDC Latency Optimisation

I. MOTIVATION

The A Large Ion Collider Experiment (ALICE) at the European Organisation for Nuclear Research (CERN) in Geneva is dedicated to the study of heavy-ion physics. It is one of the major experiments conducted at the Large Hadron Collider (LHC). The main objective of ALICE is to investigate the conditions that existed in the early universe. During the LHC Long Shutdown 2 (2019–2022), the ALICE multi-detector underwent a major upgrade, during which several significant improvements were implemented, including the installation of a new detector called the Fast Interaction Trigger (FIT). Now, the FIT detector plays an important role in CERN experiments by providing trigger signals for ALICE, as well as beam monitoring and luminosity measurements for the LHC.

For the LHC Long Shutdown 3 (LS3), an upgrade of the FIT front-end electronics (FEE) is planned. The goal of this upgrade is to extend both the precision and dynamic range of time and charge measurements. In addition, as the Texas Instruments time-to-digital converter (TDC) chips used in the current FIT front-end electronics (FEE) are no longer in production; the search for a suitable replacement has started. Meanwhile, the PicoTDC chip, newly designed at CERN, has matured into a verified device and is now available for use in future designs. Therefore, verifying the feasibility of incorporating the PicoTDC into the FIT FEE became an objective, and it is a topic of this paper. The FIT data processing latency is a crucial parameter for the FIT electronics. Unfortunately, the available PicoTDC documentation [1] does not provide sufficient information regarding PicoTDC timing characteristics, such as latency and data throughput.

As a result, a framework for simulating various PicoTDC use-case scenarios within the FIT detector was developed. An RTL model written in SystemVerilog, representing the PicoTDC chip was provided to the authors by the PicoTDC design team. The simulation testbench was configured, tuned, and extended with additional features to represent accurately FIT detector operating conditions. Through modelling, key PicoTDC timing parameters were identified, enabling the definition of appropriate configurations and operating conditions for its use in the FIT readout electronics.

This paper is organised as follows: in Section II we describe PicoTDC features. In Section III, we describe the means to achieve the desired functionality and parameters. In Section IV, the used simulation framework is explained. In section V, the findings about latency are examined. Finally, Section VI, describes how these findings correspond with the FIT detector's electronics.

This work is co-financed in part supported by the Ministry of Science and Higher Education (Agreement Nr 2023/WK/07)

Manuscript received May 22, 2026; revised July 15, 2026; accepted July 13, 2026. Published August 25, 2026.
Issue category: Special Issue on DSD/SEAA 2026 on Works in Progress (WiP) Session, Krakow, Poland, Sept. 2026.
Paper category: Short
DOI: doi.org/10.64552/wipiec.v12i2.140

II. PICOTDC INTRODUCTION

PicoTDC is a 64-channel TDC ASIC specifically designed by CERN for time-of-flight measurements in high-energy physics experiments [2]. Following the convention of the chip's manual, the term *hit* is used throughout this paper to denote an input event.

A. TDC architecture

PicoTDC is a sampling TDC based on a delay line and a resistive-capacitive interpolator. [1]. The chip operates with a 40 MHz clock, matching the standard clock frequency used across LHC experiments [3]. It features 64 input channels that are divided into four parallel groups of 16 channels each (see Fig. 1). All channels share the same counters and interpolators [1].

B. Modes of operation

PicoTDC supports two modes of operation: *single edge* and *Time Over Threshold* (TOT). The former mode outputs the absolute time of a leading edge, while the latter additionally measures the time between the leading and trailing edge. The time range is strongly tied to the frame format (see Fig. 2). The time range of the single edge mode is 204.68 µs, for TOT, there are two sub- modes, which support pulse widths up to 6.24335 ns and 777.75 ps, respectively. For the considered use case TOT mode was rejected as unsuitable.

C. Reset and time reference

An important property of the PicoTDC is the reset synchronous with the internal 320 MHz clock. Absolute time, measured by PicoTDC, is referenced to an indeterministic point in time after the reset when the counters start counting [4]. So, PicoTDC cannot be synchronised to the referenced zero time mark, and relative time data is only available.

D. Trigger Matching

Many LHC detectors take readouts only in specific time windows. Additionally, they output the time data only if the provided trigger signal is valid for a given window. For this purpose, PicoTDC has a *trigger matching* function. In PicoTDC, each measurement window corresponds to a single output data frame, and all hits outside the window are discarded during post-processing (see Fig. 3). The trigger windows may also overlap, enabling continuous readout operation. However, PicoTDC has a specific requirement that the time from the trigger signal to the beginning of the window is longer than the window length. Both quantities are multiples of 25 ns (PicoTDC internal clock is 40 MHz) [1]. The operating modes with and without the trigger matching function are called *triggered* and *triggerless*, respectively.

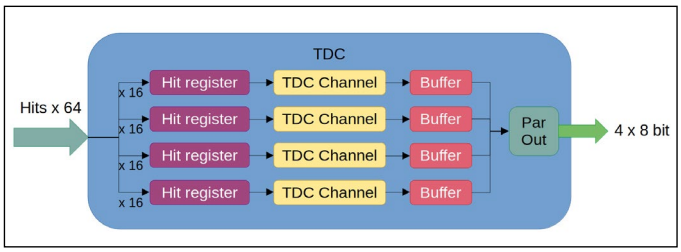

Figure 1. Simplified PicoTDC internal diagram depicting its parallel channel groups.

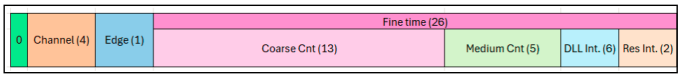

Figure 2. PicoTDC frame in single edge, triggerless mode.

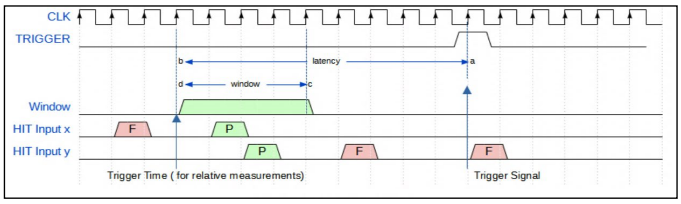

Figure 3. Trigger matching waveforms. Taken from [1].

III. CHOICE OF APPROACH

Many ALICE sub-detectors don't have the latency constraint. These detectors can aggregate hits from many bunch crossings. This allows for better utilisation of bandwidth for communication with FLP as hit data is collected with headers and trailers. PicoTDC is well-suited for this demand. PicoTDC can take data during time windows which can be much longer than a single BC period. The length of the window is configurable.

Windows of interest (later referred to as *trigger windows*) are validated by the trigger signal (see Fig. 4), which can come with the delay of the configured trigger latency.

The fundamental constraint restricted by the PicoTDC chip design is that the trigger latency shall be greater than the window width. Both the width and latency are expressed as multiples of 25 ns (period of 40 MHz LHC clock).

To optimise latency, we want to set the window duration to 25 ns and trigger latency to 50 ns. However, these parameters are not feasible because they lead to overflow of output data buffers. The output data frame consists of headers (HDR, 4 bytes), data (TDC, *number_of_hits* × *4 Bytes*) and trailer (TRL, 4 Bytes). Minimum size of frame is 12 Bytes. With the said parameters, this leads to *12 Bytes* × *40 MHz* = *480 MB/s*. Meanwhile, the PicoTDC output data rate is 320 MB/s. So the theoretical minimum latency setup configuration leads to buffer overflow. A feasible configuration is 50 ns for the window and 75 ns for the trigger latency. For this configuration, we have *12 Bytes* × *20 MHz* = *240 MB/s*. However, the latency is 155 ns, a demonstrated in Fig. 4.

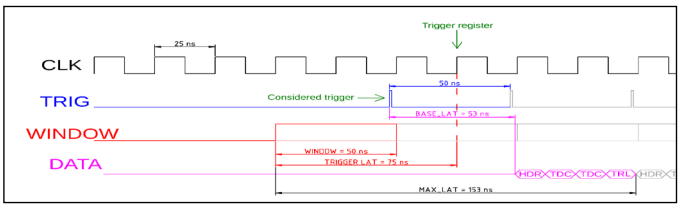

Figure 4. Trigger window, trigger latency and total latency in triggered mode. The trigger window is set to 50 ns, and the trigger latency is set to 75 ns. This is the lowest-latency valid configuration. Here, it is assumed that two hits arrived during the considered window (worst-case scenario), resulting in two TDC measurements on the data line.

This latency can be shortened if we abandon the PicoTDC triggered mode and use our custom configuration. In our proposed configuration LHC is fed into one of the PicoTDC input channels, and the relative hit time is calculated from the PicoTDC output data, but subtracting the clock time and hit time (see Fig. 5).

To verify the guaranteed latency of the designed system, a worst-case approach was chosen. This means that in the given BC, every PicoTDC channel is hit.

Latency of PicoTDC can be defined as the time elapsing from the leading edge of the first hit in BC to the trailing edge of the last bit of the last output data frame related to this BC.

IV. METHODOLOGY

The proposed idea was simulated using the PicoTDC RTL model that mimics the behaviour of the circuit in tools such as Vivado. It was kindly provided to the authors by CERN PicoTDC team member. The simulations revolved around latency.

To simply and accurately manipulate hits in the simulation model, the hit generator, from the testbench provided in the model, was replaced with a custom one that allows dividing hits among the input channels of a TDC in the later described *uniform channel allocation* manner. The new hit generator allows single-shot hits simulation for the worst-case scenario when multiple hits arrive at the inputs during the same evaluation window. The new hit generator is written in SystemVerilog and was extensively used throughout the research conducted for this work.

V. RESULTS OF LATENCY SIMULATION

A. *Evaluation window*

Our simulations show that PicoTDC collects hits before they are sent to the data output interface. The term *evaluation window* is introduced to describe this time period during which PicoTDC collects hits. The duration of this window is 12.5 ns. Also, data frames are emitted at discrete intervals corresponding to multiples of this duration - input hits are effectively grouped within 12.5 ns intervals, and the corresponding data frames are transmitted at a fixed offset relative to the start of each interval (see Fig. 6, 8).

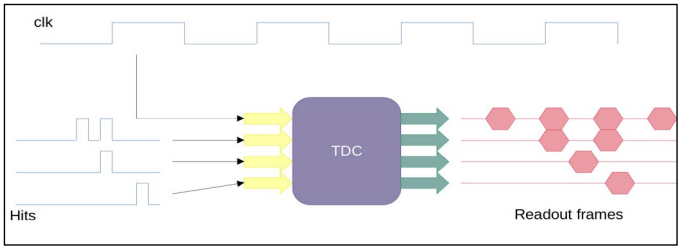

Figure 5. Proposed solution to achieve relative time measurements without using the trigger matching function.

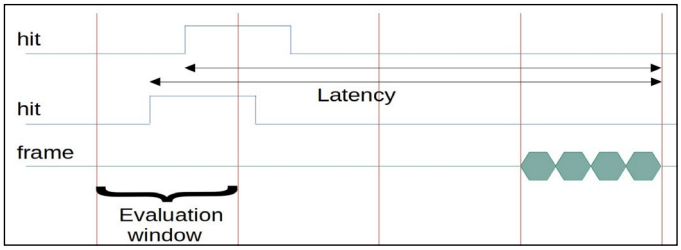

Figure 6. The figure depicts two scenarios for a single device hit. Note that the latency varies based on where the hit falls within the evaluation window.

Consequently, the latency of PicoTDC is not static - it varies because hits can happen at any time within the evaluation window. When a hit occurs just before the edge that triggers evaluation, the latency is smaller. When a hit happens further away from the edge, the latency increases. The waveform of latency over time from circuit startup is thus saw-shaped (see Figure 7).

B. *Output latency*

Total latency consists of base latency and data transmission period.

The *base output latency* (L_{base}) term refers to the interval from a hit to the beginning of the first output frame. Simulation results indicate that this latency varies between 52.5 ns and 65 ns. This is due to the relation of an incoming hit to the evaluation window.

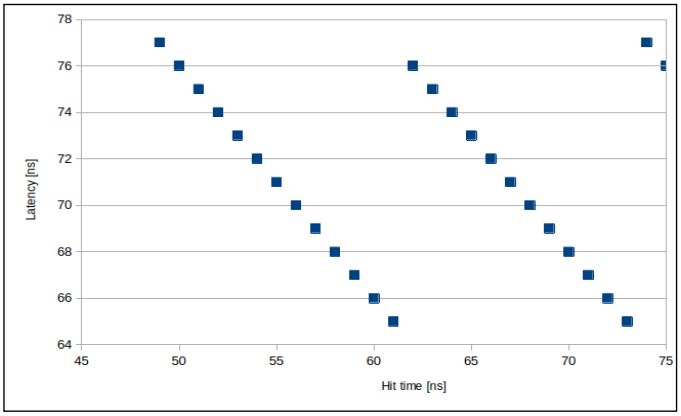

Figure 7. Latency variation forms a saw-like waveform. This pattern continues as subsequent hits arrive at the circuit inputs. The horizontal axis represents the time at which the hit arrived, from the start of the simulation.

C. *Uniform channel allocation*

As already mentioned, PicoTDC has 64 channels that are divided into four parallel channel groups of 16. Hit channels can be distributed across PicoTDC input channels in a strategic manner to minimise latency through parallelism, later referred to as uniform channel allocation (see Fig. 9, 10, 11). The number of input channels assigned to each channel group shall be equal. If the number of input channels is not divisible by the number of channel groups, the difference between maximum and minimum number of input channels assigned to each group shall not exceed 1. For N channels connected to one channel group, the maximum latency of a group can be expressed by the following equation:

$$L_{group\_max} = L_{base\_max} + N \times T_{frame}, \quad (1)$$

where L_{base_max} represents the maximum value of base output latency and T_{frame} represents the frame length.

The maximum latency of the chip in such a use case is then equal to the largest latency among the four groups.

D. *Maximum hit rate*

The maximum accepted hit rate of continuous periodic events is not given in the PicoTDC reference manual, so it was determined through analysis and simulation. While the manual states the minimum time interval between hits for them to be distinguished by the TDC at 781 ps [1], readout of hits continuously incoming with this frequency is not possible. The main limitation is the output interface throughput. Each channel group is capable of transmitting 12.5 ns long frames serially, resulting in a frame rate of 80×10^6 frames/s. Therefore, the maximum hit rate for a channel group for hits incoming constantly and periodically is 80×10^6 hits/s per channel group. A higher rate is acceptable over a short period of time until the buffers get filled.

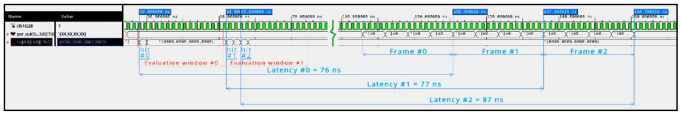

Figure 8. Example waveforms of hits in a single channel group. *clk1G28* is a simulation-only 1.28 GHz clock that defines the beginning and end of an evaluation window. *par_out* is the output interface of the chip, and hit is the 64-channel input interface. Hits 1 and 2 occur in the same evaluation window (window 1), so frame 2 must wait for frame 1, effectively increasing the latency of frame 2. Values are rounded for clarity.

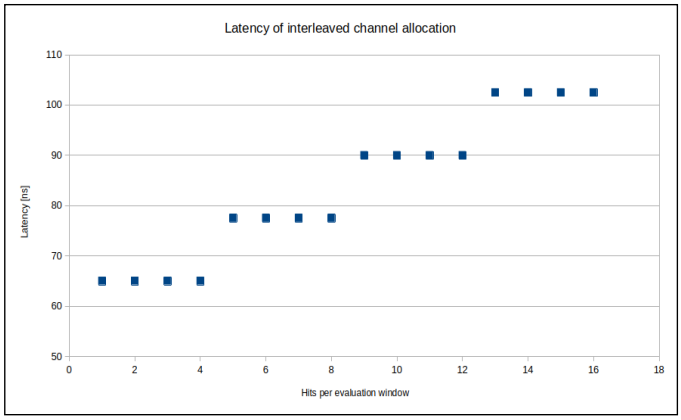

Figure 9. With uniform allocation, described in V-C, the PicoTDC processes hits in parallel across its four channel groups. Consequently, latency does not scale continuously; instead, it jumps by an additional frame length only when the total number of simultaneous hits across the chip exceeds a multiple of four (e.g., 5, 9, or 13 hits), forcing multiple channels to share the same group output. The hits' relation to the evaluation window was the same for all cases.

E. *Time reference problem*

For utilisation within FIT readout electronics, a refer- ence to the LHC clock has to be provided. The solution proposed in this paper is to connect the LHC clock to one input of the TDC. When a hit comes, a simple subtraction allows to determine the hit time relative to the clock. Then, in postprocessing, the hit can be normalised to determine its relation to the LHC clock using the following equation:

$$t_{normalised} = ((t - t_{lhc\_clk} + 0.5T) \bmod T) — 0.5T, \quad (2)$$

where t is the measured hit time, t_{lhc_clk} is the timestamp of the LHC clock measured by the TDC and T is the period of the clock. The equation is also valid in the event of counters rollover, as the 25 ns LHC clock period is below the PicoTDC time range in single edge mode (see Section II-B) and therefore it was chosen as the operating mode for the FIT FEE use case.

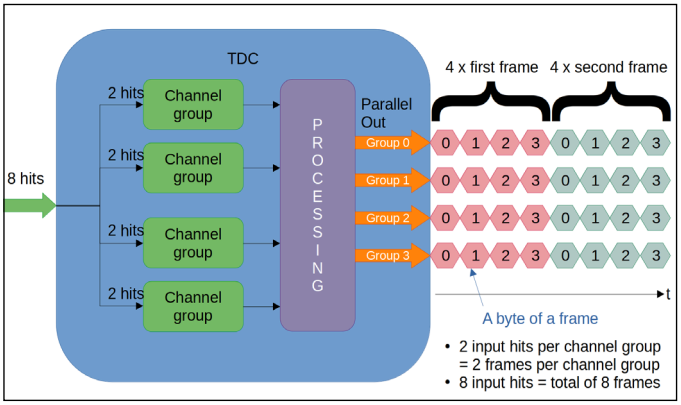

Figure 10. Utilisation of channel group parallelism with uniform channel allocation.

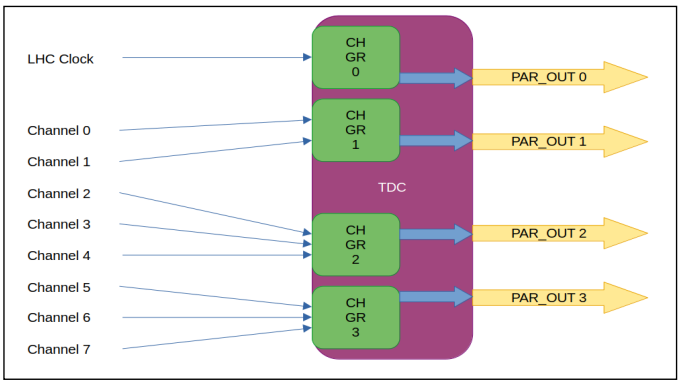

Figure 11. Uniform channel allocation for FV0. Note that channel group 0 is excluded from the input channels allocation.

Clock synchronisation timestamps must be continuously monitored. Because the signal is periodic, the frames produced by the signal will also be periodic. Since the frequency is 40 MHz, and the maximum allowed is 80 MHz; there is only space for one frame between each clock cycle. However, it cannot be guaranteed that spontaneous hits will not come in many at once, producing many frames. Many frames will result in obstruction of the clock timestamps. Then the synchronisation would fail. Therefore, it shall be assured that no hits will come to the same channel group as clock timestamps, so none of the channels in the same channel group as the clock input can be utilised. Thus, 16 channels are lost to perform this operation. This significantly reduces the latency capabilities of this solution, as only three, not four, measurements can be performed in parallel.

VI. FIT DETECTOR USE CASE

A. *FIT FEE*

FIT detector consists of three sub-detectors: FV0, FT0 and FDD. For each of them, the FEE consist of two major units: a Trigger and Clock Module (TCM) and a number of Processing Modules (PM) (see Fig. 12).

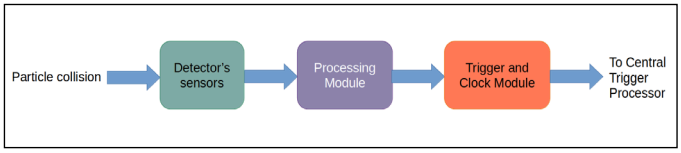

Figure 12. Simplified diagram of FIT front-end electronics

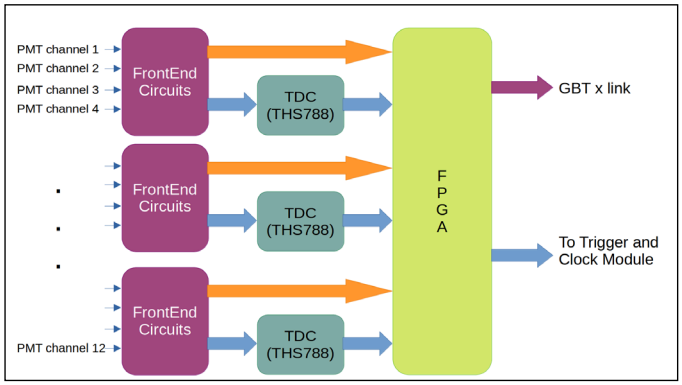

Figure 13. Simplified diagram of current, pre-upgrade, PM design. Based on: [7].

The component of FIT's electronics responsible for providing the time of the event is called a Processing Module (PM). This element features 12 channels and uses three Time to Digital Converters (TDC) to provide the time a particle hit detector's photomultipliers (PMT) to other readout systems (see Fig. 13). This work concentrated on a case study for FV0, the largest of three subdetectors of FIT, which utilises only 8 channels per PM. One of the objectives of the research was to check whether it is possible to use only a single TDC chip while maintaining the required latency.

The latency for the entire data path of FIT's readout electronics must not exceed 425 ns [5]. In this time budget, a 181 ns delay is introduced by the PMs and the rest by coaxial cables and other components [6]. A requirement was established that any replacement Time to Digital Converter must achieve a latency equal to or lower than that of the currently used THS788, measured at 116.0 ns.

B. *FV0 case study constraints*

The research revolved around an example concerning the FV0 detector. FV0 is divided into 48 sections, with each section corresponding to one data channel. These channels are then connected to 6 PMs, distributed uniformly - 8 channels are connected to each PM [7]. In the current design, there are three TDCs per PM, and four channels are connected to one TDC. Simulations were conducted to verify whether one TDC is sufficient to meet the latency requirements with all 8 input channels utilised.

C. *Proposed solution for FV0*

An example solution of uniform channel allocation, with LHC clock reference, for the FV0 use case, is depicted in the Fig. 11. FV0's 48 channels are distributed evenly among 6 PMs. The following considerations assumed a single PicoTDC chip

per PM. The simulated maximum latency for this system was 102 ns and can be expressed with an equation:

$$L_{total} = L_{base\_max} + 3 \times T_{frame}, \quad (3)$$

as there might be as many as three hits incoming at a channel group during the same evaluation window. The result of 102 ns fits within the 116 ns limit.

However, another problem arises. The maximum hit rate per channel of the readout electronics is determined by the frequency of the 40 MHz LHC clock. During each cycle, there is a 5 ns wide time window within which hits will be recorded. At maximum, there are three input channels connected to a single channel group. Assuming that every LHC cycle (40 MHz clock), a hit may come, the maximum per channel group hit rate is

$$3 \text{ hits} \times 40 \text{ MHz} = 120 \times 10^6 \text{ hits/s} \quad (4)$$

exceeding the limit of 80×10^6 hits/s. While this worst-case scenario is quite unlikely, a system like FIT cannot allow any sort of unreliability. Therefore, a single PicoTDC chip is not suitable for the use case. If two chips were used, the requirements would be fulfilled successfully. After utilising the first channel group of both TDC's for the LHC clock a total of 6 groups are left, so there will be 2 channels allocated in each group, resulting in 89.5 ns maximum latency. The findings are summed up in Table I.

TABLE I. SUMMARY OF DESIGN CONSTRAINTS AND PICOTDC-BASED SYSTEM SUITABILITY (FV0)

Configuration	*Resolution*	*Latency*	*Req. hit rate / ch group*
1× PicoTDC	3.05 ps	102 ns	120×10^6 hits/s
2× PicoTDC	3.05 ps	89.5 ns	80×10^6 hits/s

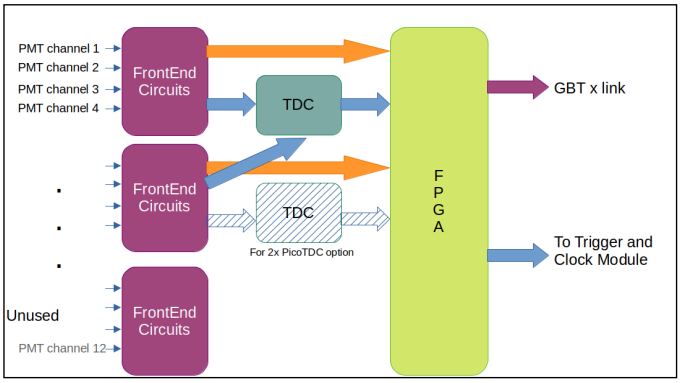

Figure 14. Simplified diagram of a PM with one or two PicoTDC chips. (FV0 use case)

VII. SUMMARY

The analysis of the PicoTDC circuit shown in this paper proved the chip to be suitable for FIT electronics upgrade in the terms of latency. However, to guarantee reliable functioning in the worst case scenario, in terms of hit rate, two chips are required for the FV0 case, but at the same time, they are capable of covering all the 12 PM channels (for other detectors than FV0). This allows scarcer input channel distribution and therefore reduces the maximum effective hit rate. However, using multiple chips significantly increases the cost. However, the integration is still possible; therefore, PicoTDC is viewed as a serious candidate for THS788 replacement.

REFERENCES

[1] CERN, picoTDC: Picosecond time to digital converter manual, CERN, Jan. 2024, for picoTDC Version 2.0.

[2] J. Christiansen, M. Horstmann, L. Perktold, and J. Prinzie, "pi- coTDC: Picosecond TDC for HEP," in IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, May 2024

[3] S. Altruda et al., "PicoTDC: A flexible 64 channel TDC with picosecond resolution," in JINST 18 P07012, 2023.

[4] CERN PicoTDC Design Team, "Private communication regarding PicoTDC architecture," Personal communication, Dec. 2024.

[5] M. Słupecki, "The fast interaction trigger for the ALICE upgrade," PhD Thesis, 2020.

[6] D. Serebryakov, "FIT electronics," Dec. 2020, presentation, CERN.

[7] ——, "FIT electronics," Apr. 2019, presentation, CERN